A UNIQUE CIRCUIT DESIGN FOR A HIGH PERFORMANCE OPERATIONAL AMPLIFIER ESPECIALLY SUITED TO MONOLITHIC CONSTRUCTION *

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INTRODUCTION

The components available in integrated circuit processes which are in production today are limited both in type and in range of values. This limitation has been more troublesome with linear integrated circuits than with digital, since many more different kinds of parts are used with conventional designs. Therefore, serious problems have arisen in adapting discrete-component designs to monolithic construction.

In many cases, an attempt has been made to develop new technology in order to integrate existing designs. This approach has met with varying degrees of success but has generally resulted in circuits which are difficult to produce in large volume. To realize a practical microcircuit with any certainty and within a reasonable period of time, it becomes necessary to use existing production technology. Fortunately, with some specialized circuit design techniques, it is possible to achieve performance with present technology which, in many cases, is equal to or better than that obtainable with discrete-component circuits. These techniques make it possible to avoid the restrictions imposed by the limited types of components, poor tolerances and the restricted range of component values. They make use of the inherent advantages of integrated circuits: close matching of active and passive devices over a wide temperature range, excellent thermal coupling throughout the circuit, the economy of using a large number of active devices, the freedom of selection of active device geometries and the availability of devices which have no exact discrete-element counterpart.

An operational amplifier which uses this circuit design philosophy is presented. It gives performance which is comparable to the best discrete component designs, yet it is relatively simple to build in monolithic form. It features low offset, high input impedance, a large input common mode range, high gain, low power consumption and a large output swing under load. The amplifier displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The suitability of the circuit for integration is indicated by the fact that it is constructed on a 55-mil-square silicon die using a six-mask planar epitaxial process which is nearly identical to that employed with common digital integrated circuits. A photomicrograph of an actual amplifier is shown in Fig. 1.

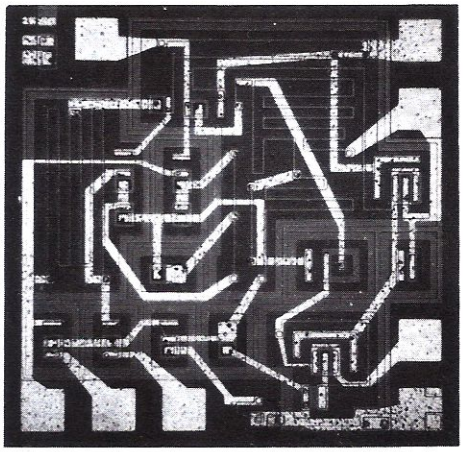

FIG. 1. Photomicrograph of the Fairchild μA709 High Performance Operational Amplifier.

INPUT STAGE

Darlington-input amplifiers have generally been used in microcircuits requiring high input impedance because of restrictions on maximum resistance values, which make it difficult to operate transistors at low collector currents. With d-c amplifiers, the Darlington connection has the disadvantage of considerably higher offset and thermal sensitivity than a non-Darlington differential pair. In addition input impedance and input currents vary as the square of the current gain with a Darlington connection, so it does not provide a great performance advantage when full temperature range operation is considered. The described design is a departure from this conventional approach: the input stage is operated at low collector currents but without requiring unusually large resistance values.

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One unusual feature of the input stage is the current source for the emitters of the input transistors which is shown in Fig. 2. It makes use of the highly predictable difference in the emitter-base voltage of two identical transistors operating at different collector currents to form a micro-ampere current source using resistances of only a few kilohms.

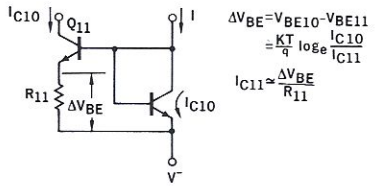

FIG. 2. Simplified Schematic of Input Stage Current Source.

With reference to Fig. 2, a relatively large current (I) is passed through the diode-connected transistor, Q_{10}. Assuming large current gains for Q_{10} and Q_{11}, the collector current of Q_{10} will be equal to this current. The emitter-base voltage of Q_{10} is used to bias the current source, Q_{11}. The resistor in the emitter of Q_{11} determines the collector current of the device.

This type of current source is described in detail in Ref. 1; but to give an example of its operation, it might be assumed that the biasing transistor (Q_{10}) is operating at 1 mA collector current and that it is desired to operate Q_{11} at 10 μA. For this ratio of collector currents, the emitter-base voltage difference between the two devices will be 120 mV at room temperature (60 mV/decade). Therefore, it is only necessary to insert a 12kΩ resistor in the emitter of Q_{11} to obtain the desired 10 μA collector current.

The differential input stage (Q_1 and Q_2) and its collector load resistors (R_1 and R_2) are shown in the complete schematic of Fig. 5. The input stage operates at approximately 20 μA collector current. The collector load resistors are relatively small for this current level, but they do provide enough gain to make the effect of second stage offset small if the second stage is reasonably well balanced.

Another interesting feature of this input stage is that the variation in current source current with temperature almost exactly compensates for the variation in input stage transconductance. As a result, the voltage gain holds constant, within a few percent, over the full operating temperature range of the circuit. In addition, the collector current of the current source is roughly proportional to the logarithm of the collector current of its biasing transistor. Since the collector current of the biasing transistor varies approximately as the supply voltage, the input stage operating level is practically unaffected by supply voltage changes.

SECOND STAGE

The second stage design is similar to that described in Ref. 2. A simplified schematic is shown in Fig. 3. The input stage collectors are connected to the bases of the second stage transistors. The collector load resistors of the input stage, R_1 and R_2, are connected as shown. In the simplified schematic, Q_6 is the second stage amplifier while Q_5 provides balanced biasing. Q_5 also serves as a unity gain inverter, delivering the full differential output of the input stage to the base of Q_6. This helps to minimize offset and thermal drift since the input stage has low gain because of the low-value collector load resistors. As pointed out in Ref. 2, this second stage design is extremely useful in going from a differential to a single ended connection in that it provides excellent isolation to variations in supply voltage when R_5 and R_6 are equal.

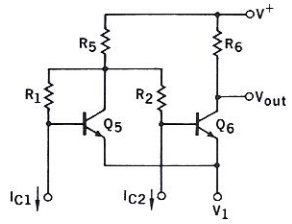

FIG. 3. Simplified Schematic of Second Stage.

The actual circuit employed is shown in Fig. 5. A modified Darlington connection is used in the second stage to prevent loading of the input stage. This makes the second stage gain proportional to the predictable transconductance characteristic of the transistors, rather than the current gain. A unique scheme is used to make the Darlington-connected second stage insensitive to high temperature leakages and stabilize it over the operating temperature range. This is shown in Fig. 4. The conventional way of accomplishing the task would be to connect a resistor across the emitter-base junction of Q_5. However, the required value of resistance would be large; and since the emitter-base voltage has a negative and the resistors a positive temperature coefficient, the bleed current would become small at high temperatures where it is needed most and large at low temperatures where it is undesirable. However, with the scheme in Fig. 4, resistance values more than an order of magnitude lower can be used and the bleed current has a strong positive temperature coefficient, as desired. As is clear from the figure, it uses the same principle as the input stage current source.

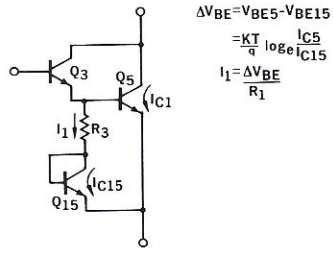

FIG. 4. Schematic Illustrating Principle of the Modified Darlington Connection.

The remaining details of the second stage are that an emitter follower, Q_7, is used to keep the input stage collector currents out of the collector of Q_5. Additionally, a second emitter follower, Q_8, is used to prevent loading of the second stage by the output stage.

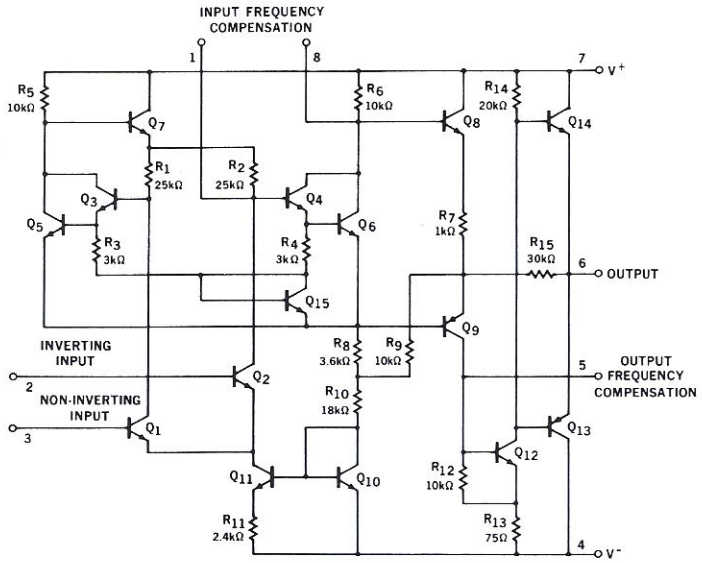

FIG. 5. Complete Schematic of the Amplifier.

OUTPUT STAGE

Level shifting to the output stage is accomplished using a lateral PNP, Q_9, similar to that described in Ref. 3. It is made using what is usually an NPN base diffusion for an emitter. This is surrounded by a second base diffusion which serves as a collector. The normal NPN collector region is then the PNP base. This structure suffers from a rather wide base, displaying a low current gain (approximately 2). However, it has the distinct advantage that it can be made with the standard NPN process with no additional steps or control. The circuit is designed to operate satisfactorily with current gains lower than 0.2, so the device presents no problem in that the PNP will work well enough as long as the junctions are good.

A complementary, class-B output stage is used. The circuit has a built-in dead zone to prevent latch-up or runaway under overload conditions; each output transistor is positively turned off before the other is allowed to conduct. However, a large amount of internal feedback, through R_{15}, is used. This not only gives a low output resistance but also makes the cross-over distortion almost indiscernible--even on the open loop transfer function. An additional advantage of this scheme is that the output stage quiescent current is held to a minimum which helps the design objective of low power consumption.

A vertical PNP is used in the output stage. This device uses the NPN base diffusion for an emitter and the P-type substrate of the integrated circuit for the collector (in the lateral PNP, this PNP action is suppressed by placing the N+ subcollector diffusion of the NPN underneath it). This PNP has a higher current gain than the lateral PNP but it also presents no problem as far as device yields are concerned since it need only function as a diode to meet circuit requirements.

Although it is not clear from the schematic, the output stage is actually short-circuit-proof. This characteristic is derived from the fact that the output transistors (Q_{14}, Q_{13} and Q_{12}) have small geometries (the whole integrated circuit is about the same size as output transistors that would normally be used). The current gain of these devices is injection efficiency limited at high current levels. The injection-efficiency-limited current gain is relatively constant for a given process and geometry and falls off at high temperatures so this turns out to be a satisfactory method of short-duration current limiting.

Other details of the output stage are that R_{12} is used to make the circuit insensitive to leakages in Q_9 and Q_{12}. R_{13} reduces the internal loop gain of the output stage to stabilize the internal feedback. The gain of the output stage is essentially determined by the ratio of R_{15} to R_7, independent of the characteristics of the active devices.

FREQUENCY COMPENSATION

Practically all operational amplifiers require frequency compensation. An example of how this is handled with an integrated operational amplifier is given in Ref. 4. Two compensation points are provided with this amplifier because of its high gain. It is difficult to get more than 60 db of compensation at one point. The points chosen have quite high transfer resistances so that the amplifier can be compensated with small external capacitors. The transfer resistance across the input frequency compensation terminals (feedback on the second stage) is 1 MΩ while the resistance across the output compensation terminals (feedback on the output stage) is 50 kΩ.

CONCLUSIONS

A circuit for an operational amplifier which is well suited for integration was described. The design makes use of the relative economy of active devices as well as complementary-transistor structures which do not complicate processing. Many of the restrictions imposed by monolithic construction were overcome on a circuit design level. While this can result in a high initial design cost, it is of great practical significance because design is a non-recurring cost in a particular microcircuit while restrictive component tolerances, extra processing steps and excessive die size represent a continuing expense in manufacture. The design requires nothing exceptional from the processing--only that the junctions be of high quality and that the transistors have current gains above a minimum value. Since these things are also required in the processing of discrete transistors, the economy of the device should be obvious.

The circuit is also quite versatile, but has a minimum of leads. This is significant with an integrated circuit both because a large number of leads creates package problems (the familiar TO-5 package becomes cumbersome to handle and use with standard printed-circuit boards if it has more than 10 leads) and because every active lead must be characterized, specified and tested.

The final proof of the design is its performance, as indicated in Table 1 and in Figs. 6 through 10, and the fact that the amplifier has been manufactured in large volume with reasonable yields. It is currently available as an off-the-shelf item from Fairchild Semiconductor.

TABLE 1

TYPICAL ELECTRICAL CHARACTERISTICS OF THE FAIRCHILD μA709 HIGH PERFORMANCE OPERATIONAL AMPLIFIER (T_A = 25°C, V_S = ±15V)

Input Offset Voltage	1 mV
Input Offset Current	50 nA
Input Bias Current	200 nA
Input Impedance	400 kΩ
Input Common Mode Range	±10 V
Common Mode Rejection	90 dB
Voltage Gain	45000
Output Voltage Swing	
R_L = 10 kΩ	±14 V
R_L = 2 kΩ	±13 V
Output Impedance	150 Ω
Power Consumption	80 mW
Power Supply Rejection	25 μV/V

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3. H. C. Lin, T. B. Tan, G. Y. Chang, B. Van Der Leest and N Formigoni, "Lateral Complementary Transistor Structure for the Simultaneous Fabrication of Functional Blocks," Proc. IEEE, Vol. 52, No. 12, pp. 1491-1495, Dec. 1964.
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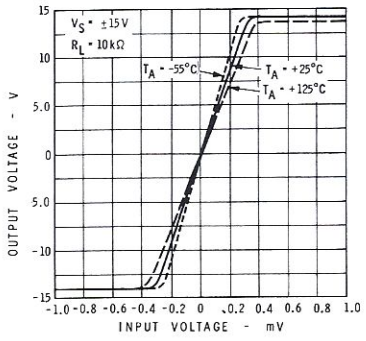

FIG. 6. Voltage Transfer Characteristic.

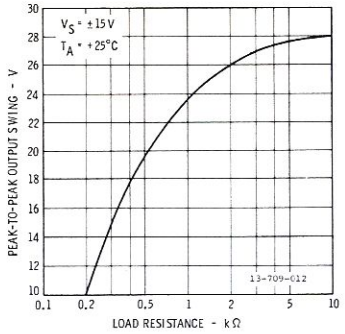

FIG. 7. Output Voltage Swing as a Function of Load Resistance.

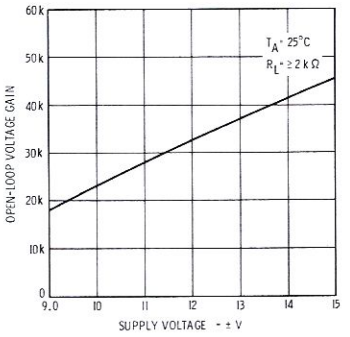

FIG. 8. Voltage Gain as a Function of Supply Voltages.

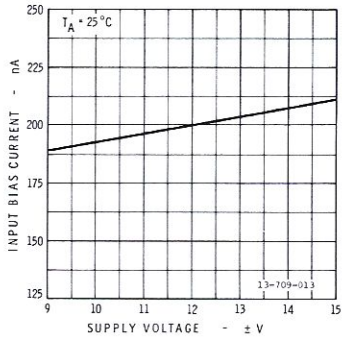

FIG. 9. Input Bias Current as a Function of Supply Voltages.

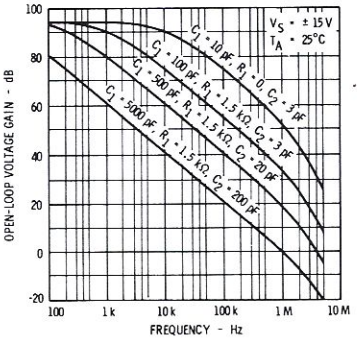
V_S = ±15V
T_A = 25°C
C_1 = 10 pF, R_1 = 0, C_2 = 5 pF
C_1 = 100 pF, R_1 = 1.5 kΩ, C_2 = 3 pF
C_1 = 500 pF, R_1 = 1.5 kΩ, C_2 = 20 pF
C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF
OPEN-LOOP VOLTAGE GAIN - dB
FREQUENCY - Hz

FIG. 10. Open Loop Frequency Response with Various Compensation Networks.